WE CLAIM:

1. A method of forming a CMOS sidewall spacer, comprising the steps of:

forming a PMOS transistor gate structure on a n-type region of a semiconductor substrate;

forming a NMOS transistor gate structure on a p-type region of said semiconductor substrate;

forming sidewall structures adjacent to said NMOS transistor gate structure and said PMOS transistor gate structure; and

etching said sidewall structure adjacent to said NMOS transistor gate structure such that the width of the sidewall structure adjacent to said NMOS transistor gate structure is less than the width of the sidewall structure adjacent to said PMOS transistor gate structure.

2. The method of claim 1 wherein said etching of said sidewall structure is an anisotropic etch.

3. The method of claim 1 wherein said sidewall structure is a material selected from the group consisting of silicon nitride, silicon oxide, and silicon oxynitride.

4. A method for forming CMOS sidewall spacers, comprising the steps of:

providing a semiconductor substrate of a first conductivity type with a region of a second conductivity type;

forming a gate dielectric on said semiconductor substrate;

forming a conductive layer on said gate dielectric;

etching said conductive layer and said gate dielectric to form a first transistor gate stack with an upper surface on said semiconductor substrate of a first conductivity and a second transistor gate stack with an upper surface on said region of said semiconductor substrate of a second conductivity type;

forming at least one first sidewall structure of a first width adjacent to said second transistor gate stack; and

forming at least one second sidewall structure of a second width adjacent to said first transistor gate stack wherein said second width is less than said first width.

5. The method of claim 4 where said forming at least one first sidewall structure of a first width comprises:

forming a sidewall film over said semiconductor substrate; and

etching said sidewall film using an anisoptropic etch such that all of said sidewall film is removed from said upper surface of said first transistor gate stack and a portion of said sidewall film is left adjacent to said second transistor gate stack.

6. The method of claim 5 where the sidewall film is silicon nitride, silicon oxide, or silicon oxynitride.

7. The method of claim 6 wherein said anisotropic etch is a plasma etch.

8. The method of claim 4 where said forming at least one second sidewall structure of a second width comprises:

providing a first transistor gate stack with at least one adjacent sidewall film of a first width;

masking said second transistor gate stack using a source drain implant mask; and

etching said sidewall film of a first width adjacent to said first transistor gate stack.

9. A method of forming a CMOS sidewall spacer method comprising the steps of:

providing a semiconductor substrate of a first conductivity type with a region of a second conductivity type;

forming a gate dielectric on said semiconductor substrate;

forming a conductive layer on said gate dielectric;

etching said conductive layer and said gate dielectric to form a first transistor gate stack with an upper surface on said semiconductor substrate of a first conductivity and a second transistor gate stack with an upper surface on said region of said semiconductor substrate of a second conductivity type;

forming a sidewall film over said semiconductor substrate;

etching said sidewall film using an anisoptropic etch such that all of said sidewall film is removed from said upper surface of said first transistor gate stack and said upper surface of said second transistor gate stack, wherein a plurality of sidewall structures of a first width are formed adjacent to said first transistor gate stack and said second transistor gate stack;

masking said second transistor gate stack with a photoresist pattern used for source drain implantation;

etching said sidewalls of a first width adjacent to said first transistor gate stack thereby forming sidewalls of a second width adjacent to said first transistor gate stack wherein said second width is less than said first width.

10. The method of claim 9 wherein said sidewall film is silicon nitride, silicon oxide, or silicon oxynitride.

11. The method of claim 9 wherein said anisotropic etch is a plasma etch.

12. The method of claim 9 wherein said first conductivity type is p-type.

13. A CMOS integrated circuit comprising:

a semiconductor substrate of a first conductivity type with a region of a second conductivity type;

a first transistor gate stack on said semiconductor substrate of a first conductivity;

a second transistor gate stack on said region of said semiconductor substrate of a second conductivity type;

sidewalls of a first width adjacent to said second transistor gate stack; and

sidewalls of a second width adjacent to said first transistor gate stack wherein said second width is less than said first width.

14. The CMOS integrated circuit of claim 13 wherein said first conductivity type is p-type.

15. The CMOS integrated circuit of claim 13 wherein said first and second transistor gate stacks comprise a dielectric layer adjacent to a conductive layer.

16. The CMOS integrated circuit of claim 14 wherein said dielectric layer is silicon oxide, silicon oxynitride or silicon nitride.

17. The CMOS integrated circuit of claim 14 wherein said conductive layer is doped silicon or a metal.

18. The CMOS integrated circuit of claim 13 wherein said sidewalls of a first width is silicon nitride, silicon oxide, or silicon oxynitride.

19. The CMOS integrated circuit of claim 13 said sidewalls of a second width is silicon nitride, silicon oxide, or silicon oxynitride.